Printed Pages – 4

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BE 5th (Semester)

Examination, April - May, 2021

Branch : IT

COMPUTER ORGANIZATION AND ARCHITECTURE

Time Allowed : Three Hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : Part (a) of each unit is compulsory and carries two marks. Attempt any two from (b), (c) or (d), each carry seven marks.

UNIT - I

Q. 1. (a) Write any two differences between linear and non linear pipeline processor.

(b) State and explain the features of Von Newmann architecture.

(c) What are various addressing modes ? Explain.

(d) Explain the structures and operational requirements of the instruction pipelines used in super scalar processor.

UNIT - II

Q. 2. (a) How are fixed point numbers represented ?

(b) Describe the floating point arithmetic operations.

(c) Explain Booth's multiplication with suitable example.

(d) Briefly explain fixed-point arithmetic addition and subtraction with signed-magnitude data.

UNIT - III

Q. 3. (a) Define the term bit-slice.

(b) Distinguish between hardwired and microprogrammed control units.

(c) List the advantages and disadvantages of hardwired control unit.

(d) Write short notes on vertical micro-programming and horizontal micro-programming.

UNIT - IV

Q. 4. (a) What is cache memory ? Write any two advantages.

(b) Describe virtual memory address space with the help of a block diagram.

(c) What is cache coherence problem ? Explain how the problem can be solved.

(d) Consider that a two-level memory system has eight virtual pages on a disk to be mapped into three page frames in the main

memory. A certain program generated the following page trace :

0, 1, 2, 4, 2, 3, 7, 2, 1, 3, 1

Compute the hit ratio using :

(i) FIFO

(ii) LRU

UNIT - V

Q. 5. (a) What is an interrupt ?

(b) Describe briefly the input-output interface.

(c) Draw the block diagram of DMA and explain the operations.

(d) Write short notes on the following in terms of network properties and routing (any two) :

(i) Node degree and Bisection width.

(ii) Perfect shuffle.

(iii) Hypercube routing.